Yuta Tokusashi

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A computer science researcher with research interests in computer architecture and data center networking and in particular power efficiency in data centers. Intersts in all layers of the system, from hardware design to Linux driver and userland applications. Experince in FPGA/VLSI and software-based co-design for highly efficient data store applications, FPGA-based DDoS mitigation and uncompressed video transmission systems.

Education

PhD candidate in Engineering, Keio University, Japan, 2016 to present

M.E. degree in Engineering from Keio University, Japan, 2016 (GPA: 3.73/4)

B.A. degree in Environmental Information from Keio University, Japan, 2014

Employment

IIJ-II Research Assistant, Jun 2013 to Feb 2017.

JST PRESTO Research Assistant, Apr 2015 to Mar 2017.

Visiting Student Researcher in The Computer Laboratory, University of Cambridge, UK, Feb 2017 to Feb 2018.

JSPS Research Fellow (DC1) Apr 2017 to present

Summer Internship at SanDisk, Western Digital (WD), Milpitas, CA, USA, Jul 2018 to Oct 2018

Programming Skills

FPGA Development using Verilog HDL

Application development using C/Ruby/Perl/Python/JavaScript

Network and Server OS:FreeBSD/Linux

Awards

“TAF Telecom System Technology Student Award” (2018)

“IPSJ Specially Selected Paper” (2016)

“IEICE CPSY Young Presentation Award” (2015)

“Best Paper Award”, The 6th International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART’15).

Excellent Engineering Prize, Digilent Design Contest 2014, World Contest, China, (2014)

First Prize, Digilent Design Contest 2014, Japan Region, Japan, (2014)

Publications

Journal Articles

Koya Mitsuzuka, Yuta Tokusashi, Hiroki Matsutani, “Efficient Message Queuing System Using FPGA-Based 10GbE Switch”, IPSJ Journal, Vol.59, No.8, pp.1446-1463, Aug 2018.

Yuta Tokusashi, Hiroki Matsutani, “Multilevel NoSQL Cache Combining In-NIC and In-Kernel Approaches”, IEEE Micro, Vol.37, No.5, pp.44-51, Sep/Oct 2017.

Ami Hayashi, Yuta Tokusashi, Hiroki Matsutani, “A Nonparametric Online Outlier Detector for FPGA NICs”, *IPSJ Journal*, Vol.56, No.8 pp.1664-1679, Aug 2016.

Yuta Tokusashi, Hiroki Matsutani, “Design of Key-Value Store Appriance Having a Variety of Data Strcture”,*IPSJ Journal*, Vol.56, No.8 pp.1787-1799, Aug 2016.

Ami Hayashi, Yuta Tokusashi, Hiroki Matsutani, “A Line Rate Outlier Filtering FPGA NIC using 10GbE Interface”, ACM SIGARCH Computer Architecture News (CAN), Vol.43, No.4, pp.22-27, Sep 2015.

Yuta Tokusashi, Yohei Kuga, Takeshi Matsuya, Osamu Nakamura, “Design and Implementation of An FPGA-Based Low-Latency HDMI Video Synchronization System”, *IPSJ Journal*, Vol.56, No.8 pp.1593-1603, Aug 2015.

Proceedings

Yuta Tokusashi, Hiroki Matsutani, Noa Zilberman, “LaKe: The Power of In-Network Computing”, Proc. of the ReConFig 2018 (To appear)

Yuma Sakakibara, Yuta Tokusashi, Shin Morishima, Hiroki Matsutani, “Accelerating Blockchain Transfer System Using FPGA-Based NIC”, Proc. of the ISPA 2018, pp.xx-xx, 2018. (To appear)

Koya Mitsuzuka, Yuta Tokusashi, Hiroki Matsutani, “MultiMQC: A Multilevel Message Queuing Cache Combining In-NIC and In-Kernel Memories”, Proc. of the FPT18, pp.xxx-xxx, Dec 2018. (To appear)

Takuma Iwata, Kohei Nakamura, Yuta Tokusashi, Hiroki Matsutani, “Accelerating Online Change-Point Detection Algorithm using 10GbE FPGA NIC”, Proc. of the 24th International European Conference on Parallel and Distributed Computing (Euro-Par18) Workshops, The 16th International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar18), pp.xxx-xxx, Aug 2018.

Yuta Tokusashi, Yohei Kuga, Ryo Nakamura, Hajime Tazaki, Hiroki Matsutani, mitiKV: An Inline Mitigator for DDoS Flooding Attacks, Proc of Internet Conference 2016, Oct 2016.

Yuta Tokusashi, Hiroki Matsutani, "NOSQL Hardware Appliance with Multiple Data Structures", Poster Session at the 28th IEEE Symposium on High Performance Chips (Hot Chips 28), Poster session, Aug 2016.

Yuta Tokusashi, Hiroki Matsutani, "A Multilevel NOSQL Cache Design Combining In-NIC and In-Kernel Caches", Proc. of the 24th IEEE International Symposium on High Performance Interconnects (Hot Interconnects'16), pp.60-67, Aug 2016.

Ami Hayashi, Yuta Tokusashi, Hiroki Matsutani, "A Line Rate Outlier Filtering FPGA NIC using 10GbE Interface", Proc. of the 6th International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART'15), Jun 2015. (**Best Paper Award**)

Workshops/Technical Report

Yosuke Yanai, Takeshi Matsuya, Yohei Kuga, Yuta Tokusashi, Jun Murai, Proposition and Implementation of RISC-V Processor with Data path extension for 10G Ethernet, IEICE Technical Reports CPSY2018, Vol.118, No.165, pp.33-38, Jul 2018.

Yuta Tokusashi, Noa Zilberman, Hiroki Matsutani, "LaKe: An Energy Efficient, Low Latency, Accelerated Key-Value Store", ACM EuroSys2018 Doctoral Workshop, Apr 2018.

Takuma Iwata, Koya Mitsuzuka, Kohei Nakamura, Yuta Tokusashi, Hiroki Matsutani, Accelerating Serialization Protocols for Network-Attached FPGAs, IEICE Technical Reports CPSY2018, Vol.117, No.378, pp.139-144, Jan 2018.

Mineto Tsukada, Koya Mitsuzuka, Kohei Nakamura, Yuta Tokusashi, Hiroki Matsutani, Accelerating Sequential Learning Algorithm OS-ELM Using FPGA-NIC, IEICE Technical Reports CPSY2018, Vol.117, No.378, pp.133-138, Jan 2018.

Yuta Tokusashi, Hiroki Matsutani, "A Cache Hierarchy in Kernel and NIC for NOSQL Acceleration", IEICE Technical Reports CPSY2015, Vol.115, No.174, pp.185-190, Aug 2015.

Yuta Tokusashi, Hiroki Matsutani, "A Case for Accelerating Data Structure Sever using FPGA NIC", IEICE Technical Reports CPSY2014-162 (ETNET'15), Vol.114, No.506, pp.1-6, Mar 2015.

Korechika Tamura, Ami Hayashi, Yuta Tokusashi, Hiroki Matsutani, "Accelerating NOSQLs using FPGA NIC and In-Kernel Key-Value Cache", IEICE Technical Reports CPSY2014-123, Vol.114, No.427, pp.7-12, Jan 2015.

Ami Hayashi, Yuta Tokusashi, Hiroki Matsutani, "An Online Outlier Detector for FPGA NICs", IEICE Technical Reports CPSY2014-124, Vol.114, No.427, pp.13-18, Jan 2015.

Yuta Tokusashi, Yohei Kuga, Takeshi Matsuya, Jun Murai, "Improving the Naturalness of Internet Video Conversation using a Low-Latency Pipeline", Proc. of Multimedia, Distributed, Cooperative and Mobile Symposium (DICOMO'13), Vol.2013, pp911-917, Jul 2013.